in untreated cells. For degradation assays, cells were incubated at 25°C for 1 hour, and receptor number (total specific ^{125}I-CYP binding sites) was determined after 24 hours of isoproterenol treatment and expressed as the percentage of receptor number assessed in nonstimulated cells. Where necessary, MG132 (20 μM) or lactacystin (20 μM) mixed in serum-free media was added to cells 1 hour before stimulation.

16. P. van Kerkhof, R. Govers, C. M. Alves dos Santos, G. J. Strous, *J. Biol. Chem.* **275**, 1575 (2000).
17. Flag epitope–tagged WT-β_2AR and β_2AR^{2-}, along with β-arrestin2, were transiently transfected in COS-7 cells with Lipofectamine. After agonist treatment, receptors were immmunoprecipitated with Flag affinity beads, and the immunoprecipitates were resolved on SDS-PAGE and probed with antibodies Ub P4D1 and β_2AR H-20.
18. W. P. Hausdorff *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **88**, 2979 (1991).
19. Confluent cells on 150-mm dishes were treated or not for 15 min with isoproterenol, after which cells were lysed in LB. Endogenous β_2AR was immunoprecipitated with the antibody β_2AR M-20. In the case of overexpressed β_2AR, cells seeded at 400,000 per 100-mm dish were transfected with pcDNA3-Flag-β_2AR plasmid using Lipofectamine, and receptor was immunoprecipitated using FLAG affinity beads (Sigma). Ubiquitinated species were detected with antibody Ub P4D1.
20. C. T. Chien, P. L. Bartel, R. Sternglanz, S. Fields, *Proc. Natl. Acad. Sci. U.S.A.* **88**, 9578 (1991).
21. S. Fang, J. P. Jensen, R. L. Ludwig, K. H. Vousden, A. M. Weissman, *J. Biol. Chem.* **275**, 8945 (2000).
22. R. Honda, H. Tanaka, H. Yasuda, *FEBS Lett.* **420**, 25 (1997).
23. For coimmunoprecipitation of endogenous proteins from whole-brain extract, brain tissue was solubilized in LB (*10*). β-Arrestin was immunoprecipitated from extracts by incubation for 4 hours at 4°C with antibody specific for β-arrestin, covalently cross-linked to Reactigel beads (Pierce). Immunoprecipitated proteins were analyzed by SDS-PAGE and detected by immunoblot analysis. For cellular experiments, COS-7 cells were transfected with COOH-terminal Flag-tagged β-arrestin and untagged Mdm2 plasmids. Flag–β-arrestins were immunoprecipitated with M2 Flag affinity beads (Sigma); the immunoprecipitates were separated by SDS-PAGE, and the presence of Mdm2 was demonstrated by immunoblotting with monoclonal antibodies (mAbs) 2A10 or AB1.
24. Supplementary Web material is available on *Science* Online at www.sciencemag.org/cgi/content/full/1063866/DC1.
25. T. Buschmann, S. Y. Fuchs, C.-G. Lee, Z-Q. Pan, Z. Ronai, *Cell* **101**, 753 (2000).
26. Recombinant β_2AR reconstituted in vesicles was used as the substrate in a ubiquitination reaction containing 20 mM Hepes (pH 7.5), 5 mM $MgCl_2$, 2 mM dithiothreitol (DTT), 2 mM adenosine 5′-triphosphate (ATP), 5 μg of ubiquitin, 20 μM MG132, and crude rabbit reticulocyte lysate (RRL, Promega), a source for the ubiquitination machinery (*36*) (5 μl/reaction). The reactions were supplemented with either His–β-arrestin2 (7 μg) or GST–β-arrestin2 (5 μg), GRK2, (1 μg), or Mdm2 [either GST-Mdm2$_{1-491}$ (8 μg) or COS-7 lysate with overexpressed Mdm2] where necessary. Reaction mixtures were incubated for 1 hour at 30°C. Ubiquitinated receptor (vesicles) was isolated by repeated washes with LB and centrifugation at 250,000*g*, 45 min. After addition of SDS–sample buffer, protein samples were incubated at 37°C for 2 hours before electrophoresis.
27. A cDNA construct of β-arrestin2 was cloned into pET-29a and was used to isolate recombinant S·TAG-β-arrestin2His6 purified on S-protein agarose beads (Novagen), which was then used as the substrate in the β-arrestin2 in vitro ubiquitination reaction containing 20 mM Hepes (pH 7.5), 5 mM $MgCl_2$, 2 mM DTT, 2 mM ATP, 5 μg of ubiquitin, 20 μM MG132, and crude RRL, either supplemented or not with 100 μg of COS cell extract (clarified by centrifugation at 21,000*g* for 15 min) with or without overexpressed Mdm2.
28. K. Nakamura, M. F. Lazari, S. Li, C. Korgaonkar, M. Ascoli, *Mol. Endocrinol.* **13**, 1295 (1999).
29. P. Tsao, T. Cao, M. von Zastrow, *Trends Pharmacol. Sci.* **22**, 91 (2001)
30. Mdm2 truncation mutants were prepared by standard polymerase chain reaction protocols and subcloned into pcDNA3. All sequences were confirmed with an automated ABI DNA sequencer (Howard Hughes Nucleic Acid Facility, Duke University).
31. J. Chen, V. Marechal, A. J. Levine, *Mol. Cell. Biol.* **13**, 4107 (1993).
32. A. L. Parola, S. Lin, B. K. Kobilka, *Anal. Biochem.* **254**, 88 (1997).
33. Flag epitope–tagged β_2ARs expressed in HEK293 cells in six-well dishes were treated with or without isoproterenol for 30 min in serum-free medium at 37°C. Cell surface receptors were labeled with Flag mAb M1, and fluorescein isothiocyanate–conjugated goat antibody to mouse immunoglobulin G was used as secondary antibody. Receptor internalization was quantified as loss of cell surface receptors, as measured by flow cytometry.
34. O. B. Goodman Jr. *et al.*, *Nature* **383**, 447 (1996).
35. S. A. Laporte *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **96**, 3712 (1999).
36. S. Mori *et al.*, *Eur. J. Biochem.* **247**, 1190 (1997).
37. M. Bouvier *et al.*, *Mol. Pharmacol.* **33**, 133 (1988).
38. We thank D. Addison, M. Holben, and J. Turnbough for secretarial assistance; B. K. Kobilka for 0-Kβ_2AR plasmid; A. J. Levine for the Mdm2 plasmid and mAb 2A10; G. Lozano for providing the Mdm2-p53 null cell line; M. Delahunty for purified rβ_2AR; W. E. Miller for pAS2 constructs and advice in yeast experiments; F. T. Lin for pcDNA3-βarrHis6 constructs; M. Cong for providing pcDNA3-β_2AR^{2-}; S. J. Perry and K. L. Pierce for critical reading; H. E. Kendall and G. P. Irons for technical assistance; W. D. Capel for purified GRK2; and G. J. Sabo for assistance. Supported by NIH grant HL16037. R.J.L is an investigator of the Howard Hughes Medical Institute.

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Logic Gates and Computation from Assembled Nanowire Building Blocks

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Miniaturization in electronics through improvements in established "top-down" fabrication techniques is approaching the point where fundamental issues are expected to limit the dramatic increases in computing seen over the past several decades. Here we report a "bottom-up" approach in which functional device elements and element arrays have been assembled from solution through the use of electronically well-defined semiconductor nanowire building blocks. We show that crossed nanowire p-n junctions and junction arrays can be assembled in over 95% yield with controllable electrical characteristics, and in addition, that these junctions can be used to create integrated nanoscale field-effect transistor arrays with nanowires as both the conducting channel and gate electrode. Nanowire junction arrays have been configured as key OR, AND, and NOR logic-gate structures with substantial gain and have been used to implement basic computation.

Fundamental physical constraints and economics are expected to limit continued miniaturization in electronics by conventional top-down manufacturing during the next one to two decades (*1*, *2*) and have thus motivated efforts world wide to search for new strategies to meet expected computing demands of the future. Bottom-up approaches to nanoelectronics (*2*), where the functional electronic structures are assembled from well-defined nanoscale building blocks, such as carbon nanotubes (*3–8*), molecules (*9–11*), and/or semiconductor nanowires (*12–14*), have the potential to go far beyond the limits of top-down manufacturing. For example, single-walled carbon nanotubes (NTs) have been used as building blocks to fabricate room-temperature field-effect transistors (FETs) (*3–5*), diodes (*6*, *7*) and recently, an inverter (*8*), which represents a key component for logic. However, the inability to control whether NTs are semiconducting or metallic (*2*, *5*) makes specific device fabrication largely a random event and poses a serious issue for integration beyond the single–device element level. A potential solution to the prob-

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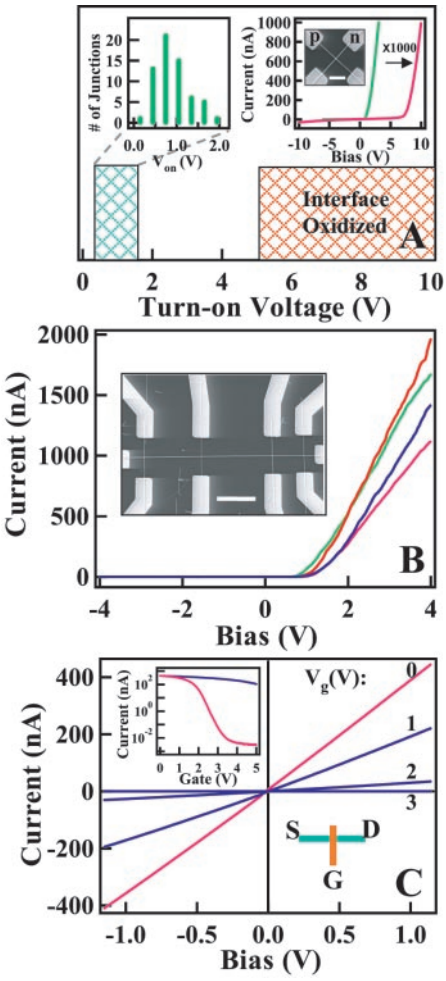

Fig. 1. Crossed NW nanodevice elements. (**A**) Turn-on voltage distribution for crossed NW junctions. The green cross-hatched area indicates the range for low turn-on voltage junctions formed from as-assembled NW junctions, and the red cross-hatched area indicates high turn-on voltage devices after local oxidation of the junction. (Top left inset) Histogram of turn-on voltage for over 70 as-assembled junctions showing a narrow distribution around 1 V. The high turn-on voltage devices have a broad distribution but generally fall into the range of 5 to 10 V. (Top right inset) An example of an *I-V* response for low (green) and high (red) turn-on voltage elements. The red curve is multiplied by 1000 for better viewing. The inset inside the top right inset shows a typical scanning electron micrograph (SEM) of a crossed NW device. Bar: 1 μm. (**B**) *I-V* behavior for a 4(p) by 1(n) multiple junction array. The four curves represent the *I-V* response for each of the four junctions and highlight reproducibility of assembled device elements. (Inset) An example of a multiple crossed NW device. Bar: 2 μm. (**C**) Gate-dependent *I-V* characteristics of a crossed NW-FET. The NW gate voltage for each *I-V* curve is indicated (0, 1, 2, and 3 V). (Top left inset) The red and blue curves show *I* versus V_{gate} for n-NW (red) and global back (blue) gates when the bias is set at 1 V. The transconductance for this device was 80 and 280 nS (V_{sd} = 1 V) when using the global back gate and NW gate, respectively. (Bottom right inset) The measurement configuration.

lem of coexisting metallic and semiconducting NTs involves selective destruction of metallic tubes (*5*), although such an approach requires extensive top-down lithography and subsequent processing to implement.

Semiconductor nanowires (NWs) have also been used as building blocks for assembling a range of nanodevices including FETs (*12*, *13*), p-n diodes (*13*, *14*), bipolar junction transistors, and complementary inverters (*14*). In contrast to NTs, these NW devices can be assembled in a predictable manner because the electronic properties and sizes of the NWs can be precisely controlled during synthesis (*12*–*15*) and methods exist for their parallel assembly (*16*). However, previous NW and NT single device elements represent only an initial step toward nanoelectronic systems, which will require both the formation of device elements and integrated device arrays in high yield. To this end, we report assembly of p-type silicon (p-Si) and n-type gallium nitride (n-GaN) NWs to form crossed nanoscale p-n junctions and junction arrays in which the electronic properties and function are controlled in a predictable manner to provide both diode and FET elements in high yield. Importantly, nanoscale p-n junction and FET arrays have been configured as OR, AND, and NOR logic gates with substantial gain, and these gates have been interconnected to demonstrate computation with a half-adder. Our approach leads naturally through the bottom-up paradigm to integration at the nanoscale and represents a step toward the creation of sophisticated nanoelectronics.

The single-crystal p-Si and n-GaN NWs used in this study were synthesized by nanocluster-catalyzed methods described previously (*14*, *15*, *17*, *18*) and had diameters of 10 to 25 and 10 to 30 nm, respectively, although NWs as small as 2 nm can be prepared (*15*). These NWs were chosen for our studies because the oxide coating on their surfaces can be independently varied (*18*) to enable good control of junction electronic properties. To demonstrate this feature, which is critical for assembly of more complex integrated devices, we have assembled and characterized the electronic properties of a large number of crossed p-Si/n-GaN junctions (*18*) (Fig. 1). Current-voltage (*I-V*) measurements show that the p-Si/n-GaN crossed NW devices exhibit current rectification characteristic of p-n diodes with a typical turn-on voltage of about 1.0 V (Fig. 1A) (*19*). These results are highly reproducible: Current rectification was observed in over 95% of the more than 70 crossed p-n NW devices studied, and in addition, 85% of the devices exhibited low turn-on voltages between 0.6 and 1.3 V (Fig. 1A, top left inset). The reproducible assembly of crossed NW structures with predictable electrical properties contrasts sharply with results from NT-based devices and has enabled us also to explore the assembly and properties of integrated p-n junction arrays. Importantly, electrical transport measurements made on a typical 4 by 1 crossed p-Si/n-GaN junction array (Fig. 1B) show that the four nanoscale cross points form independently addressable p-n junctions with clear current rectification and similar turn-on voltages. These data demonstrate the high yield and reproducibility of our crossed NW p-n devices and represent an important and necessary step for the rational assembly of more complex devices such as logic gates (see below).

In addition to these low turn-on voltage diodes, high turn-on voltage p-n junctions can be used as nanoscale FETs (Fig. 1C). Specifically, a p-channel FET with both a nanoscale conducting channel and a nanoscale gate is formed from a n-GaN/p-Si crossed NW structure; we refer to these structures as crossed NW FETs (cNW-FETs). The high turn-on voltage junctions required to assemble cNW-FETs were reproducibly formed by increasing the oxide layer thickness at the junctions by either thermal oxidation of the SiNWs (*18*) or by passing a high current through the junction in the air (*20*). Transport data recorded on over 50 p-n junctions prepared in this way (Fig. 1A) show that turn-on voltages greater than 5 V can be achieved in nearly quantitative yield, while still maintaining good conduction through individual NWs. The corresponding *I-V* data recorded on a typical cNW-FET, where the n-GaN NW is used as a nano-gate, exhibit a large decrease in conductance with increasing gate voltage (Fig. 1C) (*21*). Specifically, the conductance can be changed by a factor of more than 10^5 with only a 1- to 2-V variation in the nano-gate, whereas the conductance changes by only a factor of 10 when a global back-gate is used (Fig. 1C, top left inset). We attribute the high sensitivity of the cNW-FETs to the intrinsically thin gate dielectric between the crossed NWs, although a complete understanding of this new type of FET will require further investigation. The reproducibility, large gate response, and potential for nanoscale integration make the cNW-FETs attractive for assembling more complex electronic devices in which FETs are critical elements (*22*). In addition, these characteristics contrast recent work on NTs (*3*–*5*, *8*) that have used either global back gates, which are incompatible with independent device function, or lithographically defined local gates, which use and are constrained by conventional lithography to obtain nanoscale structures.

The high-yield assembly of crossed NW p-n junctions and cNW-FETs enables the bottom-up approach to be used for formation of more complex and functional electronic devices, such as logic gates. To demonstrate the flexibility of these NW device elements, we have investigated both diode- and FET-based

logic (*23*). First, a two-input OR gate was realized by using a 2(p) by 1(n) crossed p-n junction array with the two p-Si NWs as inputs and the n-GaN NW as the output (Fig. 2A). In this device, the output is low (logic 0) when both input voltages are low (0 V), and the output is high (logic 1) when either or both of the input voltages are high (5 V) (Fig. 2B), where a high input corresponds to forward bias of the corresponding p-n junction. The output-input (V_o-V_i) voltage response (Fig. 2B, inset) shows that V_o increases linearly with V_i when one input is set low (0 V), except for the region near 0 V. This low-response region is due to the finite turn-on voltage of the p-n junctions and produces a logic output typically 0.4 to 0.2 V less than the input voltage. Small reductions in V_o do not affect the operation of our logic gates because the low turn-on voltage contributions are reproducible and can be readily accounted for in defining the 0 and 1 states. The V_o-V_i data also show a nearly constant high output when the second input is set high (5 V). The experimental truth table for the 1 by 2 crossed NW device (Fig. 1C) summarizes the input-output response and confirms that this NW device behaves as a logic OR gate. We also note that assembly of more p-n junctions would produce a multiple input OR gate, i.e., a 1 by *n* junction array for an *n*-input OR gate.

We have also fabricated an AND gate from a 1(p-Si) by 3(n-GaN) multiple junction array (Fig. 2D). In this structure, the p-Si NW is biased at 5 V; two of the GaN NWs are used as inputs, and the third is used a gate with a constant voltage to create a resistor by depleting a portion of the p-Si NW. The logic 0 is observed from this device when either one or both of the inputs are low (Fig. 2E), because $V_i = 0$ corresponds to a forward-biased, low-resistance p-n junction that pulls down the output (logic "0"). The logic 1 is observed only when both inputs are high, because this condition corresponds to reverse-biased p-n diodes with resistances much larger than that of the constant resistor, i.e., there is a small voltage drop across the constant resistor and a high voltage is achieved at the output. The V_o-V_i data (Fig. 2E, inset) shows constant low V_o when the other input is low and nearly linear behavior when the other input is set at high. The truth table for the NW device (Fig. 2F) summarizes the input-output response and confirms that this device functions as a logic AND gate.

In addition, a logic NOR gate was assembled by using a 1(p-Si) by 3(n-GaN) cNW-FET array (Fig. 2G). The NOR gate was configured with 2.5 V applied to one cNW-FET to create a constant resistance of ~100 megohms, and the p-SiNW channel was biased at 5 V. The two remaining n-GaN NW inputs act as gates for two cNW-FETs in series. In this way, the output depends on the resistance ratio of the two cNW-FETs and the constant resistor. The logic 0 is observed when either one or both of the inputs is high (Fig. 2H). In this case, the transistors are off and have resistances much higher than that of the constant resistor, and thus most of the voltage drops across the transistors. A logic 1 state can only be achieved when both of the transistors are on, i.e., when both inputs are low. The V_o-V_i relation (Fig. 2H, inset) shows constant low V_o when the other input is high, and a nonlinear response with large change in V_o when the other input is set low. Analysis of these data and those from similar structures demonstrates that these two-input NOR gates routinely exhibit gains in excess of five, which is substantially larger than the gain reported for complementary inverters based on Si-NWs (*14*) and carbon NTs (*8*). High gain is a critical characteristic of gates because it enables interconnection of arrays of logic gates without signal restoration at each stage (*24*). The truth table for this NW device (Fig. 2I) summarizes the V_o-V_i response and demonstrates that the device behaves as a logic NOR gate. Lastly, our multiple-input logic NOR gates can function as NOT gates (simple inverters) by eliminating one of the inputs.

The predictable assembly of logic OR, AND, and NOR (NOT) gates enables the organization of virtually any logic circuit and represents a substantial advance compared with previous studies of NTs and molecular systems. First, the controllable electronic characteristics of the NW building blocks and reproducible properties of the devices assembled from these blocks contrast with the much lower control achieved to date with NTs (*3*–*8*). We believe that predictable and reproducible assembly of device elements

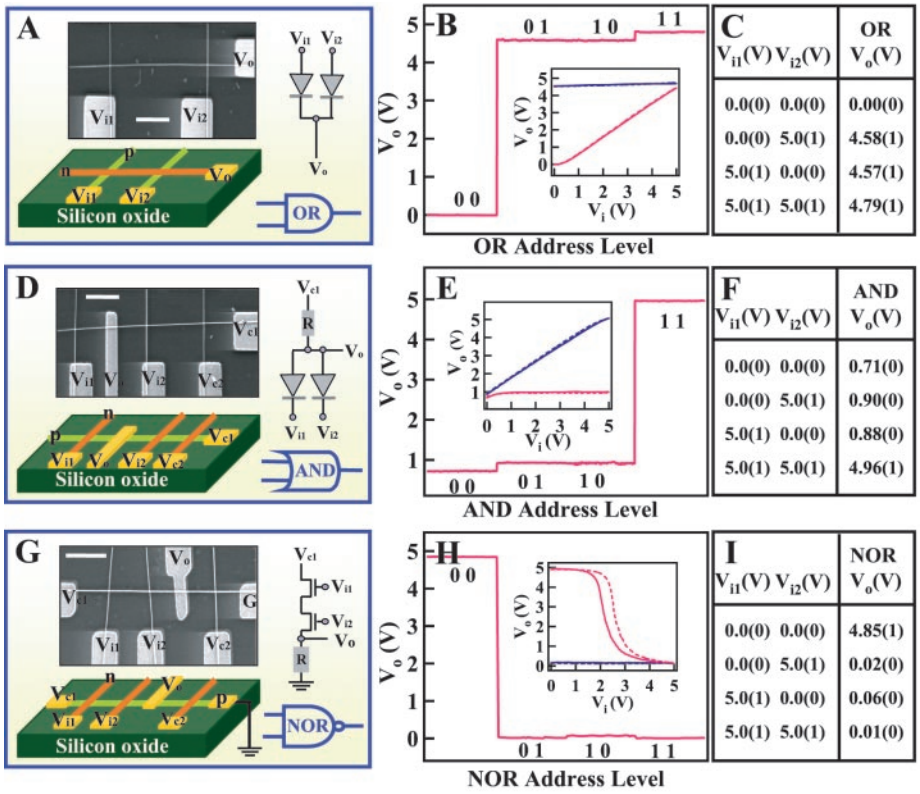

Fig. 2. Nanowire nano-logic gates. (**A**) Schematics of logic OR gate constructed from a 2 by 1 crossed NW p-n junction. (Insets) An example SEM (bar: 1 μm) of the assembled "OR" gate and symbolic electronic circuit. (**B**) The output voltage versus the four possible logic address level inputs: (0,0); (0,1); (1,0); (1,1), where logic 0 input is 0 V and logic 1 input is 5 V (same for the below). (Inset) The output-input (V_o-V_i) relation. The solid and dashed red (blue) lines show V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). (**C**) The experimental truth table for the OR gate. (**D**) Schematic of logic AND gate constructed from a 1 by 3 crossed NW junction array. (Insets) A typical SEM (bar: 1 μm) of the assembled AND gate and symbolic electronic circuit. (**E**) The output voltage versus the four possible logic address level inputs. (Inset) The V_o-V_i, where the solid and dashed red (blue) lines correspond to V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). (**F**) The experimental truth table for the AND gate. (**G**) Schematic of logic NOR gate constructed from a 1 by 3 crossed NW junction array. (Insets) An example SEM (bar: 1 μm) and symbolic electronic circuit. (**H**) The output voltage versus the four possible logic address level inputs. (Inset) The V_o-V_i relation, where the solid and dashed red (blue) lines correspond to V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). The slope of the data shows that device voltage gain is larger than 5. (**I**) The measured truth table for the NOR gate.

and arrays is especially important for integration without resorting to extensive top-down lithography to connect to those NT devices that function. Second, the use of crossed NW devices and arrays leads naturally to integration at the nanoscale and should be contrasted with NT (*3*–*5*, *8*) and molecular (*9*–*11*) devices, where the element sizes reported to date (length for NTs and area for molecules) have been determined by the same top-down lithography used in conventional electronics.

Lastly, we have interconnected multiple AND and NOR gates to implement basic computation in the form of an XOR gate (Fig. 3A), which corresponds to the binary logic function SUM, and a half adder (Fig. 3B), which corresponds to the addition of two binary bits. The XOR gate is configured by using the output from AND and NOR gates as the input to a second NOR gate, whereas the logic half adder uses an additional logic AND gate as the CARRY. The truth table for the proposed logic XOR is summarized in Fig. 3C. Importantly, the experimental V_o-V_i transport data for the XOR device (Fig. 3, D and E) show (i) that the output is logic state 0 or low when the inputs are both low or high, and logic state 1 or high when one input is low and the other is high; and (ii) that the response is highly nonlinear. The linear response region corresponds to a voltage gain of more than five and is typical of the devices measured to date. This large gain achieved in an XOR configured from CNW-FET NOR gates and a low-gain diode AND gate is due to the high gain of the cNW-FET NOR gates. We believe that further improvements in device performance could be obtained by using cNW-FET elements for all of the logic elements (*24*). Importantly, the data summarized in the experimental truth table (Fig. 3F) demonstrate that the response is that of the binary logic SUM operation, and thus that we have implemented a basic computation with the NW logic devices.

Overall, we believe that our predictable and reproducible bench-top assembly of nanoscale crossed p-n diode and cNW-FET elements and arrays, which have enabled the demonstration of all critical logic gates and basic computation, represents an important step toward integrated nanoelectronics built from primarily bottom-up versus top-down approaches. Further improvements can be made by assembling NWs directly onto predefined metal electrode arrays (*25*) and by creating more highly integrated circuit elements by feeding the output from NW to NW. Implementing these approaches could eliminate the conventional lithography used to wire-up devices in this study. In addition, in a crossbar array with 5-nm diameter NWs, it would be possible to achieve device densities approaching $10^{12}/cm^2$, which is off the present semiconductor road map for top-down manufacturing. To achieve this goal of bottom-up manufacturing in the future will require substantial work—for example, in developing much greater sophistication in assembly and further improving materials synthesis.

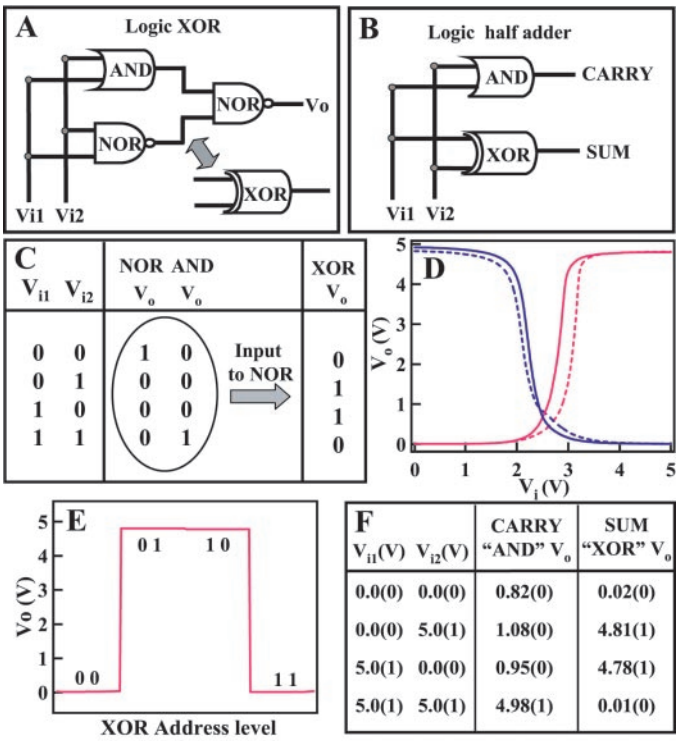

Fig. 3. Nanowire computation. (**A**) Schematic of logic XOR gate constructed with the output from an AND and a NOR as the input to a second NOR gate. (**B**) Schematic for logic half adder. (**C**) Truth table for logic XOR gate. (**D**) XOR output voltage versus input voltages. The solid and dashed red (blue) lines show V_o-V_{i1} and V_o-V_{i2} when the other input is 0 (1). The slope of the V_o-V_i data shows that the gain exceeds 10. The XOR gate was achieved by connecting the output electrodes of an AND and NOR gate to two inputs of another NOR gate. (**E**) The output voltage versus the four possible logic address level inputs for the XOR gate. (**F**) Experimental truth table for the logic half adder. The logic half adder was obtained by using the XOR gate as the SUM and an AND gate as the CARRY.

References and Notes

1. R. Compano, L. Molenkamp, D. J. Paul, *Technology Roadmap for Nanoelectronics*, European Commission IST Programme: Future and Emerging Technologies, Microelectronics Advanced Research Initiative; http://nanoworld.org/NanoLibrary/nanoroad.pdf.
2. C. M. Lieber, *Sci. Am.* (September 2001), p. 58.
3. S. J. Tans, R. M. Verschueren, C. Dekker, *Nature* **393**, 49 (1998).
4. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, Ph. Avouris, *Appl. Phys. Lett.* **73**, 2447 (1998).
5. P. G. Collins, M. S. Arnold, Ph. Avouris, *Science* **292**, 706 (2001).
6. Z. Yao, H. W. C. Postma, L. Balents, C. Dekker, *Nature* **402**, 273 (1999).
7. M. S. Fuhrer *et al.*, *Science* **288**, 494 (2000).
8. V. Derycke, R. Martel, J. Appenzeller, Ph. Avouris, *Nano Letters* **1**, 453 (2001) (Web release, 26 August 2001).
9. C. P. Collier *et al.*, *Science* **285**, 391 (1999).
10. C. P. Collier *et al.*, *Science* **289**, 1172 (2000).
11. M. A. Reed, J. Chen, A. M. Rawlett, D. W. Price, J. M. Tour, *Appl. Phys. Lett.* **286**, 1550 (2001).
12. Y. Cui, X. Duan, J. Hu, C. M. Lieber, *J. Phys. Chem. B* **104**, 5213 (2000).
13. X. Duan, Y. Huang, Y. Cui, J. Wang, C. M. Lieber, *Nature* **409**, 66 (2001).
14. Y. Cui, C. M. Lieber, *Science* **291**, 851 (2001).
15. Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, C. M. Lieber, *Appl. Phys. Lett.* **78**, 2214 (2001).
16. Y. Huang, X. Duan, Q. Wei, C. M. Lieber, *Science* **291**, 630 (2001).
17. X. Duan, C. M. Lieber, *J. Am. Chem. Soc.* **122**, 188 (2000).
18. Single-crystal p-type Si-NWs were grown by using Au nanocluster catalysts, SiH_4 reactant, and B_2H_6 dopant (SiH_4:B_2H_6, 1000:1 to 6000:1) (*15*). Single-crystal GaN-NWs were prepared by a laser-assisted catalytic growth with iron as the catalyst (target composition: GaN:Fe = 95:5) (*17*) and are naturally n-type due to nitrogen vacancies or oxygen impurities (*26*). The SiNW surfaces consist of a ~1-nm-thick amorphous oxide, which can be removed by HF etching (*14*) or increased in thickness by thermal oxidation before device assembly. The GaN-NWs have only a monolayer-thick oxide over-layer (*27*), making them ideal for forming crossed NW junctions. Stable solutions of Si-NWs and GaN-NWs were prepared by sonication in ethanol for 5 to 10 s. Individual and multiple crossed NW junctions were prepared by using a layer-by-layer fluidic alignment strategy (*16*): First, Si-NWs were aligned on the Si/SiO_2 surface from the ethanol solution by using a microfluidic channel, and crossed GaN-NWs were deposited by using the microfluidic channel oriented perpendicular to the original SiNW flow. Au/Ti electrical contacts (50 nm Ti; 70 nm Au) to the nanowires were defined by electron-beam lithography and electron-beam evaporation.
19. *I-V* measurements made on individual p-Si and n-GaN NWs in crossed NW devices show linear *I-V* behavior. The p-Si NWs have two-terminal resistances of 0.5 to 10 megohms and were determined by the SiH_4:B_2H_6 ratio (1000:1 to 6000:1) used during growth. The n-GaN NWs have two-terminal resistances of 50 to 500 kilohms.
20. The turn-on voltages of crossed NW p-n junctions were increased by Joule heating the junctions in air. Because the crossing point dominates the junction resistance (*13*, *14*), a high current will locally heat the crossing point and increase the oxide layer between crossed NWs, and thereby the junction resistance/turn-on voltage. The red line in the top right inset of Fig. 1A shows the large change in turn-on voltage after passing a 10-μA current through the junction for about 4 min; the resistance changes of the individual NWs changed less than about 10%.
21. The cNW-FET on/off ratio can vary from 10^3 to 10^5, depending on the p-Si NW carrier concentration. In

general, p-Si NWs grown with a higher dopant ratio (SiH_4:B_2H_6 = 1000:1) have lower resistance and smaller on/off ratios of ~10^3; those synthesized with a lower dopant ratio (6000:1) have higher resistance and larger on/off ratios of ~10^4 to 10^5. In addition, the carrier mobility typically varies from 30 to 200 cm^2/V-s, depending on doping.
22. S. M. Sze, *Semiconductor Devices, Physics and Technology* (Wiley, New York, 1985), pp. 208–210.
23. P. Horowitz, W. Hill, *The Art of Electronics* (Cambridge Univ. Press, Cambridge, 1989).
24. The OR and AND gates were assembled by using p-n junctions (diode logic) and do not exhibit voltage gain; however, they would show gain if implemented by using cNW-FETs. For example, logic OR can be implemented with the NOR gate by reversing the 5-V bias and ground connections to the p-Si NW. The AND function could also be implemented by using cNW-FETs in parallel (versus series for OR). In addition, we note that both p- and n-channel transistors are possible and would enable reduced power dissipation.
25. Y. Huang, X. Duan & C. M. Lieber, unpublished results.
26. J. I. Pankov, T. D. Moustakas, *Gallium Nitride* (*GaN*) *I* (Academic Press, San Diego, 1998), pp. 259–265.
27. N. J. Watkins, G. W. Wicks, Yongli Gao, *Appl. Phys. Lett.* **75**, 2602 (1999).
28. We thank H. Park for helpful discussion. C.M.L. acknowledges support of this work by the Office of Naval Research and the Defense Advanced Projects Research Agency.

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Logic Circuits with Carbon Nanotube Transistors

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We demonstrate logic circuits with field-effect transistors based on single carbon nanotubes. Our device layout features local gates that provide excellent capacitive coupling between the gate and nanotube, enabling strong electrostatic doping of the nanotube from *p*-doping to *n*-doping and the study of the nonconventional long-range screening of charge along the one-dimensional nanotubes. The transistors show favorable device characteristics such as high gain (>10), a large on-off ratio (>10^5), and room-temperature operation. Importantly, the local-gate layout allows for integration of multiple devices on a single chip. Indeed, we demonstrate one-, two-, and three-transistor circuits that exhibit a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator.

The anticipated limits to the further miniaturization of microelectronics have led to intense research directed toward the development of molecular electronics (*1*). The use of single-wall carbon nanotubes has stimulated these efforts, because these molecules exhibit a range of suitable properties for nanoelectronics. Various basic single-nanotube components have recently been demonstrated, such as molecular wires, diodes, field-effect transistors, and single-electron transistors (*2*–*8*). The next challenge in the development of molecular electronics is to go beyond single-molecule components and integrate such devices onto a chip to demonstrate digital logic operations. Here, we report such logic circuits composed of single-nanotube field-effect transistors. In addition to the realization of logic circuits, our new device layout also enables substantial electrostatic doping for modest gate voltages, which allows us to study the nonconventional screening of charge along the one-dimensional nanotubes.

Our nanotube transistors have a local gate that is insulated from the nanotube by a gate oxide layer of only a few nanometers thickness. In previous circuits, the gate consisted of an oxidized Si wafer (*6, 7, 9*), the tip of an atomic force microscope (*10*–*12*), a second nanotube (*13*), an ionic solution (*14*), or a capping Al film (*15*). The layouts of these devices do not allow integration of multiply connected devices (*16*). For example, the most popular nanotube-transistor layout uses a backgate, which applies the same gate voltage to all transistors on the chip. In contrast, our gate consists of a microfabricated Al wire with a well-insulating native Al_2O_3 layer (*17*), which lies beneath a semiconducting nanotube that is electrically contacted to two Au electrodes (Fig. 1, A and B). In this configuration, the Al_2O_3 thickness of a few nanometers is much shorter than the separation between the contact electrodes (~100 nm), enabling an excellent capacitive coupling between the gate and the nanotube. Moreover, different local Al gates can easily be patterned such that each one addresses a different nanotube transistor. This layout thus allows the integration of multiple nanotube field-effect transistors (FETs) on the same chip (Fig. 1C).

Our nanotube circuits are realized in a three-step process. First, Al gates are patterned using electron beam lithography (*18*) on an oxidized Si wafer. The insulating layer consists of the native oxide that grows by exposing the sample to air. The precise thickness of this layer is difficult to determine, but is on the order of a few nanometers (*19*). Second, single-wall carbon nanotubes produced by laser ablation are dispersed on the wafer from a dichloroethane suspension. With an atomic force microscope, those nanotubes are selected that have a diameter of about 1 nm and that are situated on top of the Al gate wires. Their coordinates are registered with respect to alignment markers. Finally, contact electrodes and interconnect wires are fabricated with electron-beam lithography by evaporating Au directly on the nanotube without an adhesion layer.

Very strong doping of the nanotube channel can be achieved with this layout (Fig. 2A) (*20*). Starting from a negative gate voltage V_g, the current I first decreases, then becomes immeasurably small, and finally increases again. This indicates that V_g shifts the Fermi level successively from the valence band (accumulation regime) to the gap (depletion), and finally to the conduction band (inversion) of the semiconducting nanotube. The nearby Al gate thus makes it possible to change the doping of the nanotube over the full range from the *p*- to the *n*-doped regime.

Our nanotube transistors can be classified as enhancement-mode *p*-type FETs (*21*), because a strong modulation of the current through the nanotube FET is possible when a small negative gate voltage is applied. The current versus bias voltage V_{sd} characteristics (Fig. 3) are typical for FETs (*22*). From the data in Figs. 2 and 3, we can extract a transconductance of our nanotube transistors of 0.3 μS and a lower limit of the on/off ratio of at least 10^5. The maximum current at which the nanotube transistor can operate is on the order of 100 nA and the on-resistance is 26 megaohms for V_{sd} = –1.3 V and V_g = –1.3 V.

For any further development of operational logic circuits, a gain (>1) at large bias voltage is a crucial requirement, because the output of one logic structure must be able to drive the input of the next logic structure. The output typically has to provide a voltage swing of about 1 V. Figure 3 indicates that in our transistors, a change in the output by more than 1 V occurs when the input voltage is changed by 0.1 V. This indicates a large-signal gain >10. A large gain combined with a large output swing can be obtained because the gate is so close to the nanotube. Our technique allows for a much larger gain than has been achieved with thick gate oxides or planar gates used in previous nanotube FETs (*6, 7, 9, 23*).

A major point of our report is that small circuits combining our nanotube transistors can be used for a variety of logic elements. Here, we describe our demonstration of an inverter, a

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